tor device according to the present invention. As is clear in comparison with the semiconductor device **11** shown in **FIG. 27, a** semiconductor device **15** of the present embodiment is characterized in that it further comprises an n− type drift layer **142** provided between the super junction structure and the n+ drain layer **100**, and the n− type drift layer **142** and the super junction structure also constitute n type drift layers. The n− type drift layer **142** is formed so as to have an impurity concentration which is lower than that of the n− type drift layer **102** in the super junction structure. Even when such an n− type drift layer **142** is provided, because the breakdown voltage is determined by the depletion of the upper super junction structure, a junction terminating regional structure can be designed as in the semiconductor devices **1** through **10** in the super junction structure described above. In the semiconductor device **15** of the present embodiment, due to the width of the p type drift layer **130** in the junction terminating region portion being made wider than that of the p type drift layer **106** in the cell region portion, the p type impurity amount of the super junction structure in the junction terminating region portion is made greater than that in the cell region portion in the same way as in the eleventh embodiment shown in **FIG. 27**. Thereby, a decrease in the breakdown voltage in the junction terminating region portion can be suppressed.

[0149] (16) Sixteenth Embodiment

[0150] **FIG. 34** is a cross-sectional view showing a schematic structure of a sixteenth embodiment of a semiconductor device according to the present invention. In the same way as in the fifteenth embodiment described above, in a semiconductor device **16** shown in **FIG. 34, n** type drift layers are constituted by the n− type drift layer **142** and the super junction structure. The n− type drift layer **142** has an impurity concentration which is lower than that of the n− type drift layer **102** in the super junction structure. In the present embodiment, as the structure of the junction terminating region portion, due to the cell pitch of the super junction structure in the junction terminating region portion being made narrower than the cell pitch in the cell region portion, the margin with respect to the concentration balance between the p type drift layer **132** and the n− type drift layer **102** can be made wider. Moreover, if the impurity amount of the p type drift layer **132** in the junction terminating region portion is made greater than that in the cell region portion, a decrease in the breakdown voltage in the junction terminating region portion can be further suppressed.

[0151] (B) Embodiment of the Method of Manufacturing Semiconductor Device

[0152] **FIGS. 35A through 35F** are schematic cross-sectional views showing one embodiment of a method of manufacturing the semiconductor device according to the present invention. The present embodiment provides a method in which the super junction structures in the respective embodiments of the semiconductor device of the present invention described above are formed by carrying out crystal growth a small number of times.

[0153] In a conventional process in which ion injection and buried crystal growth are repeated, because the p type resurf layer (p type drift layer) is formed by diffusion, the crystal growth film thickness of one time cannot be made thick. Therefore, it is necessary to repeat ion injection and buried crystal growth five to seven times. Further, as another conventional process, there is a method in which the trench groove is buried with crystal growth after the trench groove is formed. In this case, the number of buried growths can be one time. However, such buried crystal growth has been difficult because the value of the aspect ratio of the trench groove anticipated in the super junction structure is high, specifically greater than or equal to 5.

[0154] As shown in **FIGS. 35A through 35F**, the manufacturing method of the present embodiment is characterized in that a trench buried crystal growth of low aspect ratio is repeated a plurality of times. Specifically, first, a trench groove **154** whose aspect ratio is half of the aspect ratio which will be finally required is formed in the n− type semiconductor layer **151** (**FIG. 35A**), and a p-type semiconductor layer **156** is epitaxially grown so as to bury the trench groove **154** (**FIG. 35B**). Next, the p-type semiconductor layer **156** is withdrawn back until the surface of the n− type semiconductor layer **151** is exposed, and a semiconductor layer **158** buried in the trench groove is obtained (**FIG. 35C**). Thereafter, the n− type semiconductor layer is further epitaxially grown so as to cover the n− type semiconductor layer **151** and the p-type semiconductor layer **158**, and an n− type semiconductor layer **160** having a film thickness which is the same as the film thickness of the p-type semiconductor layer **158** is formed (**FIG. 35D**). Next, a trench groove **162** matching the trench groove **154** is formed in the n− type semiconductor layer **160** (**FIG. 35E**). Finally, the n− type semiconductor layer **164** is epitaxially grown so as to cover the n− type semiconductor layer **153** and the p-type semiconductor layer **158** (**FIG. 35F**). In accordance with the semiconductor device manufacturing method of the present embodiment, because buried growth can be carried out with relative easy, the super junction structure can thus be formed by a number of crystal growths which is less than that of the conventional process in which ion injection and buried crystal growth are repeated.

[0155] Note that, in the present embodiment, the super junction structure can be formed by carrying out trench buried crystal growths twice. However, the present invention is not limited thereto. For example, the trench buried crystal growth may be repeated three times or more with the aspect ratio per one time being set to one of third of a required aspect ratio. Further, if the super junction structures of the first time and the second time are formed in a striped shape and are formed so as to intersect one another, alignment can be exactly carried out.

[0156] Embodiments of the present invention have been described above. However, the present invention is not limited to these embodiments, and can be modified and achieved within the scope and the sprits thereof. For example, in the respective embodiments described above, the super junction structure, the p type base layer, the n+ source layer, and the gate electrode are formed in striped shapes. However, they may be formed so as to be in lattice shapes or staggered shapes. Furthermore, vertical power MOSFETs using silicon (Si) serving as semiconductor materials have been described. However, as other materials, for example, diamond can be used in addition to compound semiconductors such as silicon carbide (SiC), gallium nitride (GaN), aluminum nitride (AlN), or the like.